Executive Summary of the Project Completion Report

Executive Summary of the Project entitled **"Analytical Modeling and Simulations of SOI/SON MOSFETS: A Comparative Analysis to Get Better Device for Next Generation Integrated Circuits" sanctioned in favor of Prof. Subir Kumar Sarkar, Department of Electronics and Telecommunication Engineering, Jadavpur University.**

1. Most Significant achievements from the Project:

In the present era of device miniaturization, the demand for high performance devices with improved speed, reduced cost, lower power consumption and reduced size has led to the technological innovation and renovation of existing SOI/SON MOSFET structures. To attain upgraded device performance, implementation of new technologies in the existing device structures has become extremely important to successfully combat the short channel effects (SCEs) that tend to degrade the device performance due to aggressive downscaling in the nano-meter regime.

This Project mainly aims to achieve devices with upgraded performance by successfully suppressing the SCEs and thereby achieving suitable device structures that can be implemented in future generation advanced VLSI circuits.

- The innovative technologies like gate work function engineering, like the use of multi-material gate, along with channel engineering like strained silicon channel, graded channel and gate dielectric engineering like the use of a high-k gate stack structures in SOI/SON planar MOSFETs have been considered in our researches. The response towards SCEs obtained with these devices is quite satisfactory in comparison to the already existing planar SOI/SON MOSFETs. However, it has always been a prime objective in research to attain increasingly more gate control over the channel. In this context, the double gate SOI/SON MOSFETs have been introduced and incorporation of the innovative technologies in them resulted in appreciable SCE control.
- Then INTEL introduced Trigate MOSFETs/ FinFETs which come with attractive features like high-performance mobility applications, excellent immunity to SCEs, suitable adaptability to miniaturization and reduced power consumption but these structures are based on single material gate only. FinFETs offer desired gate control which we further enhanced by adding gate work function engineering technology and SON/SOI technology. The resulting structure, DMTG SON MOSFET shows upgraded performance with excellent immunity to SCEs. Furthermore, we added a work function engineered bottom gate and incorporated gate dielectric engineering and the results obtained show a desired value of threshold voltage implying high circuit speed, improved DIBL compared to the existing structures, reduced subthreshold swing ensuring reduced gate oxide leakages and reduced HCE that affirms reduced power consumption. We have also proposed a schottky based trigate MOSFET structure which exhibits excellent SCE immunity.
- Later, it has been reported that trigate MOSFETs are more trapezoidal than being rectangular. Thus it became important to study the trapezoidal FinFET behavior. We, therefore, presented the electrical behavior of a gate work function engineered trapezoidal strained channel FinFET that exhibited upgraded device features compared to the single material existing structures. All these devices have the provision of further scalability thereby meeting the demand of device miniaturization.

  In this way, we went ahead in each step finding the better device compared to the already reported devices and finally presented their characteristics that will help in realization of the characteristics of these devices before implementing them in upgraded and advanced VLSI future generation circuits.

2. Thesis Work Done:

i. PhD Thesis:

The Project Fellow has been enrolled for Ph.D, the details have been shown below in tabular form. If the financial grant for the third year could have been received from UGC then it would have helped the Project Fellow to complete the rest of her third year planned research work leading to her PhD degree.

Registration details of the Project Fellow:

Name	Thesis Title	Registration Details
Pritha Banerjee	Analytical modeling and simulation of some ultra -thin non-conventional MOSFET structures	D-7/Sc/195/18 Dated:14/03/2018

ii. **M.E/ M.Tech Thesis:** The following students have completed their P.G thesis under my guidance in the research area of the Project.

No. of M.E/ M.Tech students who completed their thesis under this Project:

Serial No.	Name	Thesis Title	Year of submission
1.	Aman Mahajan	Analytical Modeling of Gate Material and Gate dielectric Engineered Triple metal TFET	2017
2.	Tripty Kumari	Analytical Modeling and Performance Analysis Of Tunnel Field Effect Transistor with Renovated Structures	2017

iii. Publications:

Under this Project, 16 research papers [10 Journals and 6 Conference Publications] are published in peer-reviewed International journals and International Conference Proceedings [Attached in annexure A]

a. Manpower Trained:

Some of my research scholars are involved in this project and they have partially worked in the domain of the research work related to the Project. The list of the research scholars is shown below:

No. of Ph.D scholars who worked partially in the research area of the Project under the guidance of PI:

Serial No.	Name	Thesis Title	Registration Details
1.	Priyanka Saha	Analytical Modeling and Simulation of low-dimensional devices with improved performance	D-7/E/429/16 Dated 13.06.2016
2.	Dinesh Kumar Dash	Analytical Modeling based Performance Analysis of some Renovated FET structures	D-7/E/241/18 Dated: 26.04.2018

b. Publications of results:

Under this Project, 16 research papers [10 Journals and 6 Conference Publications] are published in peer-reviewed International journals and International Conference Proceedings [Attached in annexure A]

c. Other impact:

i. Impact on teaching and research:

With the completion of the project my research group has focused light on some unknown area of research. This work has enabled me and my team to provide better service to my department in the form of class room teaching, student project guidance and research guidance. Some of my other colleagues in the department have also shown interest in this area of research.

Faculty Name: Dr. Divya Somvanshi,
Department of Electronics and Telecommunication Engineering, Jadavpur University.

ii. Possibilities through this project:

The Proposed device structures may be fabricated and their performance can be validated. Further their applications in the digital circuits may be explored to investigate their performance so far speed, power consumption and area occupancy in the Integrated circuits are concerned.

iii. Plans for utilizing the facilities:

- The facilities created by this project will be used for conducting further research and offering students projects for both UG/PG levels.
- Conducting training program at University/ Institute level.

16/08/2018.

(Subir Kumar Sarkar)
Principal Investigator

Dr. Subir Kumar Sarkar
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Annexure A

List of Publications under the UGC Major Research Project:

A. Papers published under the Project (During 06.06.2016-30.06.2018)

Journals:

1. Pritha Banerjee and **Subir Kumar Sarkar**, "Modeling and Analysis of a Front High-k gate stack Dual-Material Tri-gate Schottky Barrier Silicon-on-Insulator MOSFET with a dual-material bottom gate", DOI: 10.1007/s12633-018-9940-y, accepted in Silicon, Springer **[SCI indexed, IF: 1.246]**

2. Priyanka Saha, Pritha Banerjee and **Subir Kumar Sarkar**, " 2D modeling based comprehensive analysis of short channel effects in DMG strained VSTB FET", **Superlattices and Microstructures, Elsevier**, March 2018, https://doi.org/10.1016/j.spmi.2018.03.070**[SCI indexed, IF: 2.099]**

3. Priyanka Saha, Pritha Banerjee, Dinesh Kumar Dash and **Subir Kumar Sarkar**, "Exploring the short channel characteristics of Asymmetric Junctionless Double Gate Silicon On Nothing MOSFET", accepted in **Journal of Materials Engineering and Performance, Springer**, March 2018, DOI: 10.1007/s11665-018-3281-2 **[SCI indexed, IF: 1.340]**

4. Pritha Banerjee, Priyanka Saha and **Subir Kumar Sarkar**,"Analytical Modelling and Performance Analysis of Gate Engineered Tri-gate SON MOSFET", accepted in IET Circuits, Devices & Systems, March 2018 **[SCI indexed, IF: 1.395]**

5. Pritha Banerjee and **Subir Kumar Sarkar**, "Comprehensive analysis of subthreshold short channel behavior of a Dual-material gate strained Trapezoidal FinFET", **Superlattices and Microstructures, Elsevier**, February 2018, https://doi.org/10.1016/j.spmi.2018.02.034 **[SCI indexed, IF: 2.099]**

6. Pritha Banerjee, Tripty Kumari and **Subir Kumar Sarkar**, "2-D modeling and analysis of short-channel behavior of a front high-K gate stack triple-material gate SB SON MOSFET", **Applied Physics A, Springer**, https://doi.org/10.1007/s00339-018-1567-8, January, 2018 **[SCI indexed, IF: 1.604]**

7. Pritha Banerjee, Priyanka Saha and **Subir Kumar Sarkar**,"Two dimensional analytical modeling of a high-K gate stack triple-material double gate strained silicon-on-nothing MOSFET with a vertical Gaussian doping", in **Journal of Computational Electronics, Springer**, DOI 10.1007/s10825-017-1089-1, November 2017 **[SCI indexed, IF: 1.431]**

8. Pritha Banerjee, Anup Sarkar and **Subir Kumar Sarkar**,"Exploring the short channel characteristics and performance analysis of DMDG SON MOSFET", **Microelectronics Journal**, Elsevier, Volume 67,, Pages 50-56, September 2017 **[SCI indexed, IF: 1.322]**

9. Pritha Banerjee and **Subir Kumar Sarkar**, "3-D analytical modeling of high-k gate stack dual-material tri-gate strained silicon-on-nothing MOSFET with dual-material bottom gate for suppressing short channel effects", in **Journal of Computational Electronics, Springer**, Vol.16.No.3,pp-631-639,May 2017 **[SCI indexed, IF: 1.431]**

10. Pritha Banerjee and **Subir Kumar Sarkar**, "3D Analytical Modeling of Dual Material Triple Gate Silicon-on Nothing MOSFET",**IEEE Transactions on Electron Devices**, Vol.64,Issue 2,pp-368-375,February 2017 **[SCI indexed, IF: 2.62]**

Conferences:

1. Priyanka Saha, Pritha Banerjee and **Subir Kumar Sarkar,**" 3D Modeling based performance analysis of Gate Engineered Trigate SON TFET with SiO_2/HfO_2 stacked gate oxide" in **IEEE Conference CONECCT,** organized by IEEE Bangalore Section at Hyatt Regency on16-17th , March 2018

2. Pritha Banerjee, Priyanka Saha and **Subir Kumar Sarkar,**"3-D Analytical Modeling and comprehensive analysis of SCEs of a high-K gate stack dual-material tri-gate Silicon-On-Insulator MOSFET with dual-material bottom gate", **IEEE Calcutta Conference, CALCON** 2017,Lalit Great Eastern, Dalhousie Square, Kolkata-69, 2-3rd,December 2017

3. Pritha Banerjee, Anup Sarkar, Dinesh Kumar Dash and **Subir Kumar Sarkar,** "Performance Analysis of High-K Dual Material Tri-gate SON MOSFET", **International Conference on Communication Devices and Networking (ICCDN)** 2017, Sikkim Manipal Institute of Technology, Majhitar, Sikkim, 3-4th June, 2017 **[Published as a book chapter in Advances In Communication, Devices And Networking, Lecture Notes in Electrical Engineering – Springer, DOI:https://doi.org/10.1007/978-981-10-7901-6_9 , Online ISBN: 978-981-10-7901-6]**

4. Pritha Banerjee, Aman Mahajan and **Subir Kumar Sarkar,**"3-D Analytical Modeling of Gate Engineered Tri-gate SON MOSFET", **IEEE International Conference on Devices for Integrated Circuits (DEVIC-17),**Kalyani Govt. Engg. College, 23-24 March, 2017

5. Tripty Kumari and **Subir Kumar Sarkar,** " Performance Analysis and Comparative Study of High K Triple Metal Double Gate SON TFET with SOI equivalent" IEEE International Conference on Devices for Integrated Circuits (DEVIC-17),Kalyani Govt. Engg. College, 23-24 March, 2017

6. Pritha Banerjee, Aman Mahajan and **Subir Kumar Sarkar,** "2-D Analytical Modeling of Dual-Material Double Gate Silicon-On-Nothing MOSFET", in 1st **International Conference on VLSI Device, Circuit and System (VLSI DCS 2016),** 19th-20th October,2016, Meghnad Saha Institute of Technology, Kolkata, India [Extended paper published in **Advances in Industrial Engineering and Management,** ASP, Vol. 6, No.1, 11-16,2017]

16.08.2018

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